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	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
APPLICATION NO.			TESD.0027	5469	
10/735,878	12/16/2003	Toshihiro Nakakura	11230.0027		
	590 06/16/2004		EXAM	EXAMINER	
50527	370		ARBES, CARL J		
REED SMIT	H LLP				
3110 FAIRVIE	EW PARK DRIVE, SUI	1E 1400	ART UNIT	PAPER NUMBER	
FALLS CHUR	CH, VA 22042		3729		
			DATE MAILED: 06/16/2004		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/735,878	NAKAKURA ET AL.				
Office Action Summary	Examiner	Art Unit				
	C. J. Arbes	3729				
The MAILING DATE of this communication  Period for Reply	on appears on the cover sheet wit	h the correspondence address				
A SHORTENED STATUTORY PERIOD FOR F THE MAILING DATE OF THIS COMMUNICAT  - Extensions of time may be available under the provisions of 37 ( after SIX (6) MONTHS from the mailing date of this communicat  - If the period for reply specified above is less than thirty (30) days  - If NO period for reply is specified above, the maximum statutory  - Failure to reply within the set or extended period for reply will, by Any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	TION.  CFR 1.136(a). In no event, however, may a re- ion.  s, a reply within the statutory minimum of thirty period will apply and will expire SIX (6) MON' v statute cause the application to become AB.	ply be timely filed  (30) days will be considered timely.  THS from the mailing date of this communication.  ANDONED (35 U.S.C. § 133).				
Status	•					
1) Responsive to communication(s) filed on 16 December 2003.						
<u> </u>	This action is non-final.					
Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) ⊠ Claim(s) 1-6 is/are pending in the application 4a) Of the above claim(s) is/are with 5) □ Claim(s) is/are allowed.  6) ⊠ Claim(s) 1-6 is/are rejected.  7) □ Claim(s) is/are objected to.  8) □ Claim(s) are subject to restriction	ithdrawn from consideration.					
Application Papers						
9) The specification is objected to by the Ex 10) The drawing(s) filed on is/are: a)	☐ accepted or b)☐ objected to					
Applicant may not request that any objection						
Replacement drawing sheet(s) including the 11) The oath or declaration is objected to by						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for for a) All b) Some * c) None of:  1. Certified copies of the priority docu 2. Certified copies of the priority docu 3. Copies of the certified copies of the application from the International I	uments have been received. uments have been received in A re priority documents have been Bureau (PCT Rule 17.2(a)).	pplication No received in this National Stage				
Attachment(s)  1) Notice of References Cited (PTO-892)	- 11.	Summary (PTO-413) S)/Mail Date				
Notice of Draftsperson's Patent Drawing Review (PTO-S     Information Disclosure Statement(s) (PTO-1449 or PTO Paper No(s)/Mail Date	(10)	nformal Patent Application (PTO-152)	_			

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukushima et al..

Fukushima et al teach a method for mounting a circuit board having a plurality of divided regions. A plurality of chip parts are placed into a chip parts' mounter. A transfer means moves the chip mounter to a region on the circuit board where they are to be mounted. After the housed chips are simultaneously mounted at positions on the circuit board, the circuit board is moved so that the unmounted regions of the board is placed directly beneath the chips' mounter. N.B. Near the last paragraph of Col. 4 Fukushima et al teach that a driving means for driving the circuit board or the chip transfer means can cope with a variety of patterns of the circuit board and such a manner that the traveling pitch can be freely set. If in fact Fukushima et al fail to expressly teach that an ...automatic mounting range step is such the automatic mounting range is set within a predetermined range on a single original board... it is held that this limitation or step would have been obvious to an artisan, given the evidence provided by Fukushima et al. (It is also noted that Fukushima et al is aware of using a compute with a stepping motor (Cf. Col 4, lines 56ff). As applied to Claims 3 and 4 wherein the circuit board is used as a main circuit board for a TV receiver, the Patent office responds that it is circuit boards are universally used today as means for

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providing electrical circuits for TV receivers. Hence it would have been obvious to use the circuit boards produced by Applicants' method to provide TV receivers. As applied further to Claim 3 it is held to mere design choice to rotate main circuit board 180 degrees to obtain a second area which is coincident with a first area. Applicants provide no specific purpose therefore nor do they articulate and specific problem solved thereby.

Any inquiry concerning this communication should be directed to C. J. Arbes at telephone number (703)308-1857.

CARL J. ARBES PRIMARY EXAMINER